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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,856	08/29/2003	Bernd Goller	MAS-FIN-403	9446
24131	7590	04/22/2005	EXAMINER	
LERNER AND GREENBERG, PA			IM, JUNGHWA M	
P O BOX 2480			ART UNIT	
HOLLYWOOD, FL 33022-2480			PAPER NUMBER	
			2811	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/651,856

Applicant(s)

GOLLER ET AL.

Examiner

Junghwa M. Im

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 and 31-41 is/are pending in the application.
- 4a) Of the above claim(s) 1-23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 24-29 and 31-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 31-32 and 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 31 and 40 recites "the active surface being embedded in said first plastic layer," and at least one wiring structure disposed above said second plastic layer. The instant invention, in particular, in Figures 9-11 which the pending claim intends to recite shows at least one wiring structure disposed below on the first plastic layer, in detail, at least one wiring structure is in contact with the first plastic layer, not with the second plastic layer.

Claims 32 and 41 are dependent on the rejected base claim.

Claim 39 recited an unclear limitation of "said wiring structure has an adhesive layer on interfaces to a plastic plate formed by said first and second layers." The instant invention does not disclose that the wiring structure has an adhesive layer.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 24-29 and 31-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6515355), hereinafter Jiang in view of Takeuchi et al. (US 6548598), hereinafter Takeuchi.

Regarding claim 24, Fig. 9A of Jiang shows an electronic component with a semiconductor chip, comprising:

- a multilayer plastic embedding compound [12', 24', 56] embedding the semiconductor chip [20'], said multilayer compound forming a first plastic layer [56] and a second plastic layer [12'; a plastic substrate]

- the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

- the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

- said first plastic layer surrounding the semiconductor chip;

- said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

- said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

- said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

- at least one wiring structure [22' or conductive trace] disposed above said second plastic layer, said wiring structure having through-contacts [54] between contact regions of the semiconductor chip and external contacts of the electronic component [through a solder ball 14'].

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

Regarding claim 25, it is intrinsic that Fig. 9A of Jiang shows said first plastic layer is formed with a plastic embedding compound having different levels of crosslinking staggered vertically, with a highest level of crosslinking being arranged in a region of a base surface of said first plastic layer since the first plastic layer is treated to form a crosslinked siloxane network [col. 3, line 60- col. 4, line 4]. In addition, note that "crosslinking staggered vertically and crosslinking being arranged" are a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 26, it is intrinsic that Fig. 9A of Jiang shows said first plastic layer is formed with a plastic embedding compound having a completely crosslinked region at a base plate and a precrosslinked region thereabove through forming a crosslinked siloxane as discussed in claim 25.

Regarding claims 27 and 28, Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46], therefore, the spherical particles forming spacers for the semiconductor chips in the first plastic layer and having a uniform predefined diameter through being a glass bead.

Art Unit: 2811

Regarding claim 29, Jiang discloses that said second plastic layer has a polyimide resin forming a leveling compensating compound [col. 2, lines 54-55]. Also, note that "forming a leveling compensating compound" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 31, insofar as understood, Fig. 9A of Jiang shows an electronic component with an electronic component with a semiconductor chip, comprising:

a multilayer plastic embedding compound [12', 56, 24'] embedding the semiconductor chip [20'], said multilayer compound forming a first plastic layer [56] and a second plastic layer [12'];

the semiconductor chip having an active surface and a passive surface, the active surface being embedded in said first plastic layer [12'];

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

at least one wiring structure [22' or conductive trace] disposed above said first plastic layer, said wiring structure having through-contacts [54] between contact regions of the

Art Unit: 2811

semiconductor chip and external contacts of the electronic component [through the electrodes 14'].

Fig. 9A of Jiang shows substantially the entire claimed structure except "said first plastic layer having a bead." Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

Regarding claim 32, insofar as understood, Fig. 9A of Jiang shows the active surface of the semiconductor chip [20'] projects from said first plastic layer [56].

Regarding claim 33, Fig. 9A of Jiang shows a portion of a blank with a plurality of component positions for electronic components, each having at least one semiconductor chip, the blank comprising:

- a first plastic layer [56] surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

- a second plastic layer [12'] above said first plastic layer, said first plastic layer having an upper boundary to said second plastic layer;

- the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

- said first plastic layer surrounding the semiconductor chip

- said second plastic layer resting on regions of the marginal sides of the semiconductor chips not covered by said first plastic layer;

Art Unit: 2811

a further component plane defined above said second plastic layer, and said second plastic layer having a level upper side forming an interface to said further component plane [through a solder ball 14'];

wiring structures [22' or conductive trace] with through-contacts [54] between contact regions of the semiconductor chips and external contacts of electronic components disposed above at least one of said second plastic layer and the semiconductor chips;

at least one of said first and second plastic layers being at least partly cured [col. 3, line 24 – col. 4, line 40] and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate.

Fig. 9A of Jiang shows substantially the entire claimed structure except “said first plastic layer having a bead.” Takeuchi discloses adding glass beads to the thermoplastic resin which is the identical plastic material in the first plastic layer of the instant invention [col. 7, lines 32-46].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Takeuchi into the device of Jiang in order to have the first plastic layer filled with glass beads to form a denser plastic layer.

The subject matters regarding claims 34 and 35 have been discussed in claims 25 and 26 concurrently.

The subject matters regarding claims 36-38 have been discussed in claims 27-29 concurrently.

Regarding claim 39, insofar as understood, Fig. 9A of Jiang shows said wiring structure is covered by adhesive material [24; epoxy] on interfaces to a plastic plate formed by said first and second layers.



Art Unit: 2811

Regarding claim 40, insofar as understood, Fig. 9A of Jiang shows a portion of a blank which forms a plurality of component positions for electronic components, each having at least one semiconductor chip [18], the blank comprising:

- a first plastic layer [56] surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

- a second plastic layer [12'] above said first plastic layer, said first plastic layer having an upper boundary to said second plastic layer;

- the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

- the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

- said first plastic layer surrounding the semiconductor chip;

- said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

- said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

- a further component plane defined above said second plastic layer, and above said second plastic layer having a level upper side forming an interface to said further component plane;
- wiring structures [22' or conductive trace] with through-contacts [54] between contact regions of the semiconductor chips and external contacts of the electronic component [through a solder ball 14'] disposed at least one of second plastic layer and semiconductor chips [Fig. 7].

Art Unit: 2811

at least one of said first and second plastic layers being at least partly cured [col. 3, line 24 – col. 4, line 40] and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate.

Regarding claim 41, insofar as understood, Fig. 9A of Jiang shows the active surface of the semiconductor chip [20'] projects from said first plastic layer [56].

### *Response to Arguments*

Applicant's arguments filed January 25, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims. And below are the Examiner's remarks in response to Applicant's argument.

Applicant argues, "Jiang et al. discloses an FR4 board and a siloxane coating. Neither of these material is a plastic embedding compound." First, it is noted an FR4 board and siloxane are plastic compound. And furthermore, it is pointed out that Jiang et al. explicitly discloses that a semiconductor chip is embedded partially in a PPMS layer [56] and a plastic substrate [12'].

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2811

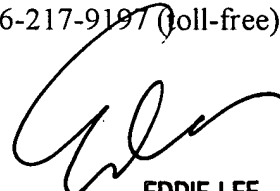
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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